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Fast hardware-software coverification by optimistic execution of real processor

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Abstract:

To achieve fast verification of the software part of an embedded system, we propose to run the target processor optimistically, which effectively reduces the synchronization overhead with other simulators. For the optimistic processor execution, we present a processor execution platform and state saving/restoration methods. We performed optimistic execution of ARM710A processor in the coverification of an IS-95 CDMA cellular phone system and obtained up to one order of magnitude higher performance compared with the case that the processor was conservatively

Index Terms:

application specific integrated circuits embedded systems formal verification hardware-software codesign integrated circuit design synchronisation ARM710A processor IS-95 CDMA cellular phone system embedded system hardware-software coverification optimistic execution processor execution platform real processor state saving/restoration methods synchronization overhead target processor

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ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers

Ing-Jer Huang Tai-An LuInst. of Comput. & Inf. Eng., Nat. Sun Yat-Sen Univ., Kaohsiung;*This paper appears in: Design Automation Conference, 1999. Proceedings*
36th06/21/1999 -06/25/1999, 1999Location: New Orleans, LA, USAOn page(s): 580-5851999References Cited: 17IEEE Catalog Number: 99CH36361Number of Pages: xxxii+1003INSPEC Accession Number: 6496041**Abstract:**

This paper presents a synthesis tool ICEBERG for embedded in-circuit emulator (ICE's), that are part of the development environment for microcontroller (or microprocessor)-based systems (PIPER-II). The tool inserts and integrates the necessary in-circuit emulation circuitry into a given RTL core of a microcontroller and thus turning the core into an embedded ICE. The ICE, based on the IEEE 1149.1 JTAG architecture, provides standard debugging mechanisms, including boundary scan paths, partial scan paths, single stepping, internal resource monitoring and modification, breakpoint detection, and mode switching between debugging and free running modes. ICEBERG has been successfully applied to synthesize the embedded ICE for an industrial microcontroller HT48100 from RTL core

Index Terms:

boundary scan testing computer debugging computer testing development systems level synthesis logic testing microcontrollers virtual machines HT48100 ICEBERG 1149.1 JTAG architecture PIPER-II RTL core boundary scan paths breakpoint detection debugging mode development environment embedded in-circuit emulator synthesizer running mode internal resource modification internal resource monitoring microcontroller microprocessor-based systems mode switching partial scan paths single stepping standard debugging mechanisms synthesis tool

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